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10/621,364	07/18/2003	Toshihiro Yanagi	12480-000018US	4032

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,364	YANAGI ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Request for Continued Examination filed on the 26 June 2006. Claims 1-16 are pending.

Response to Arguments

2. Applicant's arguments filed the 26 June 2006 have been fully considered but they are not persuasive.

On page 12, final paragraph the applicant begins the argument for the amended claims 1, 4-6 and 12. In the applicant's argument, the applicant argues that the combination of the references AAPA, Miyajima and Ranganathan fails to teach a display device including a "driving control circuit," which generates "a control clock signal based on at least a base clock signal," and a clock signal generation circuit for "generating a clock signal," where "the base clock signal, the clock signal and the control clock signal have different speeds." The applicant continues on page 13, second and third paragraphs to state that Miyajima determines the ENA signal based upon a master clock MCLK, however, since Miyajima fails to teach that the speed of the enable signal ENA is different from the speed of the master clock signal MCLK that the timing control 160 cannot constitute the "driving control circuit," of claim 1. The applicant then states in the final paragraph of page 13 that since AAPA and Ranganathan also fail to teach

this limitation of the claim that the combination of the three references fails to teach claim 1 as amended. The examiner respectfully disagrees.

Since the rejection is based upon the combination of the three references, even assuming that the enable signal and the MCLK signal of Miyajima do not have different speeds (which the examiner does not admit is true), AAPA is used to teach that the clock signals can have different speeds. So although none of the references individually teach the limitation as claimed, the combination of the references does teach the claimed limitations.

On page 14, second paragraph the applicant argues the examiner's rebuttal in the April 13, 2006 advisory action by saying that the examiner used hindsight in saying that the references could be combined based on the fact that the display device of claim 1 did not include a limitation directed to how the length of the inaction period is determined. The examiner respectfully disagrees.

The examiner's rebuttal was in response to the applicant's argument that the references could not be combined because the references could not determine how long the circuits were turned off for if the clock was turned off. The examiner was only saying that it was not pertinent that the rejection state how the length inaction period was determined in the references because it was not claimed. The examiner would like to point the applicant's attention then to Figure 5 of Ranganathan and column 9, lines 25-58 where it is explained that when the driving circuits are turned off the CLK signal is ceased to be sent to the active circuits and that the timing is kept with CLKSRC.

Ranganathan therefore can determine the length of the inaction period because there is always a clock signal that is present. This feature of Ranganathan, as stated in the advisory action, was not needed in the rejection because the claims did not state that there had to be a way to determine the inaction period.

On page 15 the applicant begins the argument of claims 2, 3, 7-11 and 13-16 in stating that the combination of the references used do not teach of the newly amended claims because the claims teach of generating at least one of output timing clock, the start timing clock and the control clock signal (each of which are different in speed).

With regards to this argument the examiner respectfully disagrees for the same reasons as stated above with regards to claims 1, 4-6 and 12, in that the rejection is based upon the combination of the three references, and although none of the references individually teach the limitation as claimed, the combination of the references does teach the claimed limitations.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the base clock signal must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figures 12-13 and Page 4 line 10 to Page 5 line 16 of the specification) in view of Miyajima et al. (US 2002/0140661) and further in view of Ranganathan (US 5,615,376).

Regarding claim 1, APA discloses a display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display (Page 4, line 25 to Page 5, line 5) comprising:

a driving control circuit (Figure 12, item 109).

APA fails to teach of a display device comprising:

a driving control circuit which

(a) generates, as a driving control signal, a control clock signal that defines an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which

(b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period; and

a clock generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control signal.

Miyajima et al. disclose a display device comprising:

a driving control circuit (Figure 1, item 100) which

(a) generates, as a driving control signal, a control clock signal (Figure 2, PANEL CONTROL SIGNAL) based on at least a base clock signal (Figure 2 and paragraph [0026] explain that the timing controller 160 generate the timing signals based on the clock signal MCLK.), the control clock signal defining an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen (Paragraphs [0043]-[0044]. The examiner interprets that through the PANEL CONTROL SIGNAL line shown in Figure 2 the ENB signal is outputted which is output during an inaction-period and is a specific length in time, therefore making it define an inaction period and a control clock signal.), and which

(b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period (Paragraph [0031]. The examiner interprets that since the outputs of the H and V drivers are stopped that this is stopping the driving of the circuits.); and

a clock generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control signal (Figure 2, Timing Control 160. The examiner interprets that the Timing Controller 160 generates clock signals since it is stated in paragraph [0026] that the T/C 160 produces and supplies timing signals necessary for each of the circuits. Paragraph [0039] and Figure 5, show a clock signal CKH1 used for taking the data signal into the data line which is faster than the ENB signal.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to using the driving control circuit taught by Miyajima et al. with the display device taught by the APA in order to produce an active matrix type liquid crystal display in which the power consumption is reduced and, at the same time, necessary and sufficient voltage can be applied to the liquid crystals.

APA and Miyajima et al. fail to teach of a display device where the driving control circuit stops driving of the clock generation circuit in an inaction period, in addition to stopping driving of the driving circuits.

Ranganathan discloses a display device where the driving control circuit stops driving of the clock generation circuit in an inaction period, in addition to stopping driving of the driving circuits (Column 3, lines 2-15 and Column 4, lines 66-67. The examiner interprets that pausing of the clock stated in column 3 would consist of stopping driving of the clock since in column 4, lines 66-67 it is stated that clocking of circuitry is disabled.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the idea of stopping the driving of the clock circuit as taught by Ranganathan with the display device taught by the combination of APA and Miyajima et al. in order to create a method for conserving power by managing the various clocks and to disable them when they are not needed.

APA also discloses of DCK, Hsync and a Vsync clock signals each of which has a different speed with the DCK clock having a faster timing than both of the Hsync and a Vsync (Figure 13 shows the clock DCK has a faster timing that the Hsync and Vsync

clocks, where the Hsync and Vsync clocks have different timings, meaning that all of the clocks have different timings.), which, based on the previous modification and combination of APA, Miyajima et al. and Ranganathan, would apply to making the base clock signal, the clock signal and the control clock signal all have different timings.

Regarding claim 4, please refer to the rejection of claim 1, and furthermore APA also discloses the display device wherein: the clock signal generation circuit is a clock signal oscillation circuit for oscillating a clock signal (Figure 12, item 106), and APA also discloses of DCK, Hsync and a Vsync clock signals each of which has a different speed with the DCK clock having a faster timing than both of the Hsync and a Vsync (Figure 13 shows the clock DCK has a faster timing that the Hsync and Vsync clocks, where the Hsync and Vsync clocks have different timings, meaning that all of the clocks have different timings.), which, based on the previous modification and combination of APA, Miyajima et al. and Ranganathan, would apply to making the base clock signal, the clock signal and the control clock signal all have different timings.

Regarding claim 5, APA, Miyajima et al. and Ranganathan disclose the display device as set forth in claim 1. APA also teaches of liquid crystal display elements being used as the pixels (Page 4, lines 10-19).

Regarding claim 6, this claim is rejected under the same rationale as claim 1.

Regarding claim 12, APA, Miyajima et al. and Ranganathan disclose the display device as set forth in claim 1. Miyajima et al. also disclose wherein:

the clock signal generation circuit generates the clock signal based on the control clock signal generated by the driving control circuit (The examiner interprets that since the clock generation circuit is T/C 160 as described above, and that since the control clock signal is also generated in T/C 160 located in the control circuit, that the clock signal generated by the clock signal generation circuit is generated based on the control clock signal generated by the same circuit.).

6. Claims 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figure 12 and Page 4 line 10 to Page 5 line 16 of the specification) in view of Miyajima et al. (US 2002/0140661) and further in view of Ranganathan (US 5,615,376) and Chee (US 6,088,806).

Regarding claim 2, please refer to the rejection of claim 1, and furthermore APA, Miyajima et al. and Ranganathan fail to teach of the display device further comprising:

an output timing clock generation circuit for generating an output timing signal of a driving signal to the display section from the driving circuits, wherein:

the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit, and the driving

control circuit stops driving of the output timing clock generation circuit in the inaction period

Chee discloses the display device further comprising:

an output timing clock generation circuit for generating an output timing signal of a driving signal to the display section from the driving circuits, wherein: the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit, and the driving control circuit stops driving of the output timing clock generation circuit in the inaction period (Column 4, lines 64-67 and Column 5, lines 1-5. The examiner interprets that since the power-down circuitry is capable of sending an enable/disable signal to the clock generator and that the clock generation circuit is then able either to send or not to send a clocking signal to the circuitry of the monitor, that it would contain an output timing clock generation circuit to create the timing that the clock generation circuit would then send to the monitor.) .

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the clock circuitry taught by Chee with the display device taught by the combination of APA, Miyajima et al. and Ranganathan in order to separate different circuits and to selectively supply power to them when needed in order to reduce power consumption.

APA also discloses of DCK, Hsync and a Vsync clock signals each of which has a different speed with the DCK clock having a faster timing than both of the Hsync and a Vsync (Figure 13 shows the clock DCK has a faster timing that the Hsync and Vsync clocks, where the Hsync and Vsync clocks have different timings, meaning that all of the

clocks have different timings.), which, based on the previous modification and combination of APA, Miyajima et al., Ranganathan and Chee would apply to making the output timing clock, the clock signal and the control clock signal all have different timings.

Regarding claim 7, this claim is rejected under the same rationale as claim 2.

7. Claims 3, 8-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figure 12 and Page 4 line 10 to Page 5 line 16 of the specification) in view of Miyajima et al. (US 2002/0140661) and further in view of Ranganathan (US 5,615,376), Chee (US 6,088,806) and Tsuda et al. (US 2002/0180673).

Regarding claim 3, please refer to the rejection of claim 2, and furthermore APA, Miyajima et al., Ranganathan and Chee fail to teach of the display device further comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits, wherein:

the output timing clock generation circuit generates the output timing clock based on the start timing clock generated in the start timing clock generation circuit, and the driving control circuit stops driving of the start timing clock generation circuit in the inaction period.

Tsuda et al. disclose a display device comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits (Paragraph [0107]. The examiner interprets that since the gate driver starts scanning in response to a gate start pulse signal receiver from the control IC, that the control IC contains a start timing generation circuit to create the signal. The examiner also interprets that when combined with the circuits taught by the combination of APA, Miyajima et al., Ranganathan and Chee that this gate start pulse signal, start timing signal, would cause the clock enabling signal to be sent to the output timing clock and that during the inaction period the power-down circuitry would also stop the driving of the start timing clock generation circuit based on the control clock signal, the control IC.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the circuitry taught by Tsuda et al. with the display device APA, Miyajima et al., Ranganathan and Chee in order to provide a matrix-type display device and a driving method thereof which permits the power consumption to be reduced to a sufficient level while ensuring basic display quality such as brightness, contrast, response speed, gradation, etc. can be realized.

APA also discloses of DCK, Hsync and a Vsync clock signals each of which has a different speed with the DCK clock having a faster timing than both of the Hsync and a Vsync (Figure 13 shows the clock DCK has a faster timing that the Hsync and Vsync clocks, where the Hsync and Vsync clocks have different timings, meaning that all of the clocks have different timings.), which, based on the previous modification and

combination of APA, Miyajima et al., Ranganathan, Chee and Tsuda et al. would apply to making the start timing clock, the clock signal and the control clock signal all have different timings.

Regarding claim 8, APA, Miyajima et al., Ranganathan and Chee disclose the display device as set forth in claim 7.

APA, Miyajima et al., Ranganathan and Chee fail to teach of the display device further comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits, wherein:

the start timing dock generation circuit generates the start timing clock based on the output timing clock generated in the output timing clock generation circuit.

Tsuda et al. disclose a display device comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits (Paragraph [0107]. The examiner interprets that since the gate driver starts scanning in response to a gate start pulse signal receiver from the control IC, that the control IC contains a start timing generation circuit to create the signal. The examiner also interprets that when combined with the circuits taught by the combination of APA, Miyajima et al., Ranganathan and Chee that this gate start pulse signal, start timing signal, would be generated based on the output timing clock.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the circuitry taught by Tsuda et al. with the display device APA, Miyajima et al., Ranganathan and Chee in order to provide a matrix-type display device and a driving method thereof which permits the power consumption to be reduced to a sufficient level while ensuring basic display quality such as brightness, contrast, response speed, gradation, etc. can be realized.

Regarding claim 9, APA, Miyajima et al., Ranganathan, Chee and Tsuda et al. disclose the display device as set forth in claim 8, wherein: the driving control circuit generates the control clock signal based on the start timing clock generated by the start timing clock generation circuit (The examiner interprets that through the combination of the teachings of APA, Miyajima et al., Ranganathan, Chee and Tsuda et al. that the driving control circuit would generate the control clock based on the start timing clock.).

Regarding claim 10, this claim is rejected under the same rationale as claim 3.

Regarding claim 11, APA, Miyajima et al., Ranganathan, Chee and Tsuda et al. disclose the display device as set forth in claim 10, wherein: the driving control circuit generates the control clock signal based on the start timing clock generated by the start timing clock generation circuit (The examiner interprets that through the combination of the teachings of APA, Miyajima et al., Ranganathan, Chee and Tsuda et al. that the driving control circuit would generate the control clock based on the start timing clock.).

Regarding claim 13, APA, Miyajima et al. and Ranganathan disclose the display device as set forth in claim 12.

APA, Miyajima et al. and Ranganathan fail to teach of a display device comprising:

the output timing clock generation circuit generates the output timing clock from the control clock signal generated by the driving control circuit

Chee discloses a display device comprising an output timing clock generation circuit (Column 4, lines 64-67 and Column 5, lines 1-5. The examiner interprets that since the power-down circuitry is capable of sending an enable/disable signal to the clock generator and that the clock generation circuit is then able either to send or not to send a clocking signal to the circuitry of the monitor, that it would contain an output timing clock generation circuit to create the timing that the clock generation circuit would then send to the monitor. The examiner interprets that under the combination of APA, Miyajima et al., Ranganathan and Chee that the output timing clock generation circuit would have to generate its signal based on some kind of action received from the circuitry of the monitor and that the action would most likely be receiving the control clock signal used to control the clocks.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the clock circuitry taught by Chee with the display device taught by the combination of APA, Miyajima et al. and Ranganathan in order to

separate different circuits and to selectively supply power to them when needed in order to reduce power consumption.

APA, Miyajima et al., Ranganathan and Chee fail to teach of a display device comprising:

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits.

Tsuda et al. disclose a display device comprising a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits (Paragraph [0107]. The examiner interprets that since the gate driver starts scanning in response to a gate start pulse signal receiver from the control IC, that the control IC contains a start timing generation circuit to create the signal.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the circuitry taught by Tsuda et al. with the display device APA, Miyajima et al., Ranganathan and Chee in order to provide a matrix-type display device and a driving method thereof which permits the power consumption to be reduced to a sufficient level while ensuring basic display quality such as brightness, contrast, response speed, gradation, etc. can be realized.

Regarding claim 14, this claim is rejected under the same rationale as claim 2.

Regarding claim 15, this claim is rejected under the same rationale as claim 8.

Regarding claim 16, this claim is rejected under the same rationale as claim 11.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

AMR A. AWAD
PRIMARY EXAMINER

14 July 2006